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M. Tech I Year I Semester (Theory-4, Lab-2, MC-1, SE-1, AC-1)							
Sl. No.	Category	Course Code	Course Title	Hours per week			Credits
				L	T	P	C
1.	PC	25MEV01T	CMOS Digital IC Design	3	0	0	3
2.	PC	25MEV02T	Microcontrollers and Programmable Digital Signal Processors	3	0	0	3
3.	PE	25MEV03T 25MEV04T 25MEV05T	**Program Elective-I:** 1.Communication Buses and Interfaces 2.Data Acquisition System Design 3.FPGA Architectures and Applications	3	0	0	3
4.	PE	25MEV06T 25MEV07T 25MEV08T	**Program Elective-II:** 1.Low Power VLSI Design 2.Scripting Languages for VLSI 3.Network Security and Cryptography	3	0	0	3
5.	PC	25MEV01P	CMOS Digital IC Design Lab	0	0	4	2
6.	PC	25MEV02P	Microcontrollers and Programmable Digital Signal Processors Lab	0	0	4	2
7.	MC	25MMC01	Research Methodology and IPR	2	0	0	2
8.	SE	25MSE01 25MSE02	RTL Synthesis, Simulation and Verification **(OR)** IoT and RTOS for Embedded Applications	0	1	2	2
9.	AC	25MAC01 25MAC02 25MAC03	**Audit Course – I** 1.Technical Research paper writing 2.Disaster Management 3.Essence of Indian Traditional Knowledge	2	0	0	0
Total				**16**	**1**	**10**	**20**

K. Sravan kumar
MEMBER SECRETARY

Head of the Department
Dept. of Electronics & Communication Engg.
GEETHANJALI INSTITUTE OF SCIENCE & TECHNOLOGY
GANGAVARAM (V), Kovur (M)
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M. Tech I Year I semester

CMOS DIGITAL IC DESIGN					
Course Code	**L:T:P:S**	**Credits**	**Exam marks**	**Exam Duration**	**Course Type**
25MEV01T	**3:0:0:0**	**3**	**CIE:30 SEE:70**	**3 Hours**	**PC**

Course Objectives:

- To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
- The course also involves analysis of performance metrics.
- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

Syllabus	**Total Hours: 45**
Unit-I	**9 Hrs**

MOS Design Pseudo NMOS Logic: Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

Unit-II	**9 Hrs**

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

Unit –III	**9 Hrs**

Sequential MOS Logic Circuits: Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

Unit –IV	**9 Hrs**

Dynamic Logic Circuits: Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

Unit –V	**9 Hrs**

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

Textbooks:

1. Neil Weste, David Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”, 4th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011

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M. Tech I Year I semester

2. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, AnanthaChandrakasan, Borivoje Nikolic, 2ndEdition, PHI

Course Outcomes(CO):

On completion of this course, student will be able to:

CO1: Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS.

CO2: Estimate Delay and Power of Adders circuits.

CO3: Classify different semiconductor memories.

CO4: Analyze, design and implement combinational and sequential MOS logic circuits.

CO5: Analyze complex engineering problems critically in the domain of digital IC design for conducting research.

CO6: Solve engineering problems for feasible and optimal solutions in the core area of digital ICs.

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MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Course Code	L:T:P:S	Credits	Exam marks	Exam Duration	Course Type
25MEV02T	3:0:0:0	3	CIE:30 SEE:70	3 Hours	PC

Course Objectives:

- To learn about ARM Microcontroller architectural features
- To understand the ARM 'C' Programming for various applications
- To study the DSP processor fundamentals and its development tools

Syllabus	Total Hours: 45

Unit-I — **9 Hrs**

ARM Cortex-Mx Processor: Applications, Programming model – Registers, Operation - modes, Exceptions and Interrupts, Reset Sequence, Instruction Set (ARM and Thumb), Unified Assembler Language, Memory Maps, Memory Access Attributes, Permissions, Bit-Band Operations, Unaligned and Exclusive Transfers. Pipeline, Bus Interfaces.

Unit-II — **9 Hrs**

Exceptions, Types, Priority, Vector Tables, Interrupt Inputs and Pending behaviour, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, Basic Configuration, SYSTICK Timer, Interrupt Sequences, Exits, Tail Chaining, Interrupt Latency

Unit –III — **9 Hrs**

LPC 17xx microcontroller- Internal memory, GPIOs, Timers, ADC, UART and other serial interfaces, PWM, RTC, WDT.

Unit –IV — **9 Hrs**

Programmable DSP (P-DSP) Processors: Harvard architecture, Multi port memory, architectural structure of P-DSP- MAC unit, Barrel shifters, Introduction to TI DSP processor family

Unit –V — **9 Hrs**

VLIW architecture and TMS320C6000 series, architecture study, data paths, cross paths, Introduction to Instruction level architecture of C6000 family, Assembly Instructions memory addressing, for arithmetic, logical operations.

Textbooks:

1. Joseph Yiu, "The definitive guide to ARM Cortex-M3", Elsevier, 2nd Edition
2. Venkatramani B. and Bhaskar M. "Digital Signal Processors: Architecture, Programming and Applications", TMH, 2ndEdition.

Reference Books:

1. Sloss Andrew N, Symes Dominic, Wright Chris, "ARM System Developer's Guide: Designing and Optimizing", Morgan Kaufman Publication.
2. Steve furber, "ARM System-on-Chip Architecture", Pearson Education

Course Outcomes(CO):

On completion of this course, student will be able to:

CO1: Learn about ARM Microcontroller architectural features.
CO2: Understand the ARM 'C' Programming for various applications.
CO3: Apply knowledge of microcontroller for Embedded system design.
CO4: Study the DSP processor fundamentals and its development tools.
CO5: Understand architecture of DSP Processor.
CO6: Integrate knowledge of embedded processor architectures and peripherals to design efficient real-time and DSP-based embedded applications

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COMMUNICATION BUSES AND INTERFACES

Course Code	L:T:P:S	Credits	Exam marks	Exam Duration	Course Type
25MEV03T	3:0:0:0	3	CIE:30 SEE:70	3 Hours	PE-I

Course Objectives:

- To understand the concepts of different types of serial buses.
- To learn about CAN, PCIe and USB architecture
- To learn about data streaming using serial communication protocols

Syllabus	Total Hours: 45

Unit-I	9 Hrs

Serial Busses- Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features, Limitations and applications of RS232, RS485, I2C , SPI.

Unit-II	9 Hrs

CAN ARCHITECTURE- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Data frame, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

Unit –III	9 Hrs

PCIe: Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

Unit –IV	9 Hrs

USB: Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration- Device detection, Default state, Addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver.

Unit –V	9 Hrs

Data streaming Serial Communication Protocal- Serial Front Panel Data Port(SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable.

Textbooks:

1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.
2. Serial Port Complete-COM Ports, USB Virtual Com Portsand Ports for Embedded Systems- Jan Axelson, Lakeview Research, 2nd Ed.,

Reference Books:

1. USB Complete – Jan Axelson, Penram Publications.
2. PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.

Course Outcomes(CO):

On completion of this course, student will be able to:

CO1: Understand the concepts of different types of serial buses.
CO2: Learn about CAN architecture.
CO3: Learn about PCIe architecture.
CO4: Learn about USB architecture.
CO5: Learn about data streaming using serial communication protocols.
CO6: Integrate knowledge of multiple serial communication protocols to evaluate and select suitable interfaces for real-time embedded system applications.

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DATA ACQUISITION SYSTEM DESIGN					
Course Code	**L:T:P:S**	**Credits**	**Exam marks**	**Exam Duration**	**Course Type**
25MEV04T	**3:0:0:0**	**3**	**CIE:30 SEE:70**	**3 Hours**	**PE-I**

Course Objectives:

- To understand the different types of communication interface buses.
- To familiarize different methods of ADC's and DAC's characteristics, specifications
- To study the software tools to develop the code and implementation for data acquisition system

Syllabus	**Total Hours: 45**
Unit-I	**9 Hrs**

Fundamentals of Data Acquisition Systems, Sensors and Transducers, Signal conditioning - Introduction, Types of signal conditioning, Classes of signal conditioning, DAQ Hardware, DAQ Software, Communications Cabling, Parameters of a DAQ System.

Unit-II	**9 Hrs**

Data acquisition system configuration, Computer plug in I/O, Distributed I/O, Stand-alone or distributed loggers/controllers- Introduction, Methods of operation, Stand-alone logger/controller hardware, firmware & software design, Communications hardware interface, Host software, Considerations, internal systems, USB overall structure, PCMCIA card

Unit –III	**9 Hrs**

Data Acquisition Systems: Hardware-Introduction, Plug-in DAQ Systems, Converters A/D, Converters D/A, Amplifier, Multiplexer/De-multiplexer, Power Management, Timing System, Filtering, Memory Board, Bus Interface.

Unit –IV	**9 Hrs**

Communication Bus-Bus and FireWire, Serial Communications, Wireless, Ethernet and Bluetooth, GSM for Data Acquisition System, PCI and PCI Express, Standard VME.

Unit –V	**9 Hrs**

Design of Data Acquisition System: Introduction to the Design, Functional Design of high-Speed Computers-Based DAS, Portable DAS, Design Guidelines for High-Performance Multichannel. Software for Data Acquisition Systems, Introduction to Lab VIEW, Android for DAQ, Design of Firmware, Example of Implementation of Software.

Textbooks:

1. Maurizio Di Paolo Emilio "Data acquisition systems-from fundamentals to applied design" springer, 2013.
2. John Park and Steve Mackay "Practical Data acquisition for instrumentation and control systems" Elsevier, 2003..

Reference Books:

1. Robert H King, "Introduction to Data Acquisition with Lab VIEW", 2nd edition, 2012, McGraw

Course Outcomes(CO):

On completion of this course, student will be able to:

CO1: Understand the fundamentals of Data Acquisition System.

CO2: Understand the different types of communication interface uses.

CO3: Familiarize different methods of ADC's characteristics, specifications.

CO4: Familiarize different methods of DAC's characteristics, specifications.

CO5: Study the software tools to develop the code.

CO6: Implement software coding for data acquisition system.

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FPGA ARCHITECTURES AND APPLICATIONS					
Course Code	**L:T:P:S**	**Credits**	**Exam marks**	**Exam Duration**	**Course Type**
25MEV05T	**3:0:0:0**	**3**	**CIE:30** **SEE:70**	**3 Hours**	**PE-I**

Course Objectives:

- To acquire knowledge about various architectures and device technologies of PLD's.
- To comprehend FPGA Architectures.
- To analyze System level Design and their application for Combinational and Sequential Circuits.
- To familiarize with Anti-Fuse Programmed FPGAs.
- To apply knowledge of this subject for various design applications

Syllabus	**Total Hours: 45**
Unit-I	**9 Hrs**

Introduction to Programmable Logic Devices: Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

Unit-II	**9 Hrs**

Field Programmable Gate Arrays: Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

Unit –III	**9 Hrs**

SRAM Programmable FPGAs: Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

Unit –IV	**9 Hrs**

Anti-Fuse Programmed FPGAs: Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

Unit –V	**9 Hrs**

Design Applications: General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

Textbooks:

1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.

Reference Books:

1. Field Programmable Gate Arrays-John V. Oldfield, Richard C. Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/Samiha Mourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier, Newnes.
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series

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Course Outcomes(CO):

On completion of this course, student will be able to:

CO1: Acquire knowledge about various architectures and device technologies of PLD's.

CO2: Comprehend FPGA Architectures.

CO3: Analyze System level Design and their application for Combinational Circuits.

CO4: Analyze System level Design and their application for Sequential Circuits.

CO5: Familiarize with Anti-Fuse Programmed FPGAs.

CO6: Apply knowledge of this subject for various design applications.

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LOW POWER VLSI DESIGN					
Course Code	**L:T:P:S**	**Credits**	**Exam marks**	**Exam Duration**	**Course Type**
25MEV06T	**3:0:0:0**	**3**	**CIE:30 SEE:70**	**3 Hours**	**PE-II**

Course Objectives:

- To understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect.
- To implement Low power design approaches for system level and circuit level measures.
- To design low power adders, multipliers and memories for efficient design of systems.

Syllabus	**Total Hours: 45**
Unit-I	**9 Hrs**

Fundamentals: Need for Low Power Circuit Design, Sources of Power Dissipation – Static and Dynamic Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects – Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect

Unit-II	**9 Hrs**

Low-Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

Unit –III	**9 Hrs**

Low-Voltage Low-Power Adders: Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

Unit –IV	**9 Hrs**

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introduction to Wallace Tree Multiplier

Unit –V	**9 Hrs**

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

Textbooks:

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

Reference Books:

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2. Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.

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3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

Course Outcomes(CO):

On completion of this course, student will be able to:

CO1: Understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect.

CO2: Implement Low power design approaches for system level measures.

CO3: Implement Low power design approaches for circuit level measures.

CO4: Design low power adders for efficient design of systems.

CO5: Design low power multipliers for efficient design of systems.

CO6: Design low power memories for efficient design of systems.

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SCRIPTING LANGUAGES FOR VLSI					
Course Code	**L:T:P:S**	**Credits**	**Exam marks**	**Exam Duration**	**Course Type**
25MEV07T	**3:0:0:0**	**3**	**CIE:30 SEE:70**	**3 Hours**	**PE-II**

Course Objectives:

- Learn programming with scripting languages
- Understand how to create and run scripts using PERL/TCL/PYTHON in CAD Tools
- Gain knowledge about PERL/PYTHON/ TCL in developing system and web applications
- Develop skill to design a real time project using PERL/PYTHON

Syllabus	**Total Hours: 45**
Unit-I	**9 Hrs**

Introduction to Scripts and Scripting: Basics of Linux, Origin of Scripting languages, scripting today, Characteristics and uses of scripting languages.

Unit-II	**9 Hrs**

PERL: Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Collections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments.

Unit –III	**9 Hrs**

Advanced PERL: Finer points of Looping, Subroutines, Using Pack and Unpack, working with files, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects and modules in action, tied variables, interfacing to the operating systems, Security issues.

Unit –IV	**9 Hrs**

TCL: The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/output, Procedures, Working with Strings, Patterns, Files and Pipes, Example code.

Unit –V	**9 Hrs**

Advanced TCL: The eval, source, exec and up-level commands, Libraries and packages, Namespaces, Trapping errors, Event-driven programs, Making applications 'Internet-aware', 'Nuts-and-bolts' internet programming, Security issues, TCL and TK integration.
PYTHON: Introduction to PYTHON language, PYTHON-syntax, statements, functions, Built-in functions and Methods, Modules in PYTHON, Exception Handling.

Textbooks:

1. The World of Scripting Languages- David Barron, Wiley Student Edition.
2. PYTHON Web Programming, Steve Holden and David Beazley, New Riders Publications

Reference Books:

1. TCL/TK: A Developer's Guide- Clif Flynt, Morgan Kaufmann Series.
2. Core PYTHON Programming, Chun, Pearson Education.
3. Learning Perl, Randal L. Schwartz, O' Reilly publications 6th edition.
4. Linux: The Complete Reference", Richard Peterson McGraw Hill Publications, 6th Edition.

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Course Outcomes(CO):

On completion of this course, student will be able to:

CO1: Gain fluency in programming with scripting languages
CO2: Create scripts using PERL/TCL/PYTHON in CAD Tools
CO3: Run scripts using PERL/TCL/PYTHON in CAD Tools
CO4: Demonstrate the use of PERL/PYTHON/ TCL in developing system applications
CO5: Demonstrate the use of PERL/PYTHON/ TCL in developing web applications
CO6: Develop a real time project using PERL/PYTHON.

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NETWORK SECURITY AND CRYPTOGRAPHY					
Course Code	**L:T:P:S**	**Credits**	**Exam marks**	**Exam Duration**	**Course Type**
25MEV08T	**3:0:0:0**	**3**	**CIE:30 SEE:70**	**3 Hours**	**PE-II**

Course Objectives:

- To identify and utilize different forms of cryptography techniques.
- To incorporate authentication and security in the network applications.
- To distinguish among different types of threats to the system and handle the same.

Syllabus	**Total Hours: 45**
Unit-I	**9 Hrs**

Security: Need, security services, Attacks, OSI Security Architecture, one-time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

Unit-II	**9 Hrs**

Number Theory: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

Unit –III	**9 Hrs**

Private-Key (Symmetric) Cryptography: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

Unit –IV	**9 Hrs**

Public-Key (Asymmetric) Cryptography: RSA, Key Distribution and Management, DiffieHellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

Unit –V	**9 Hrs**

Authentication and System Security: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer, Secure Electronic Transaction Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Trusted Systems.

Textbooks:

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2ND Edition

Reference Books:

1. Christopher M. King, ErtemOsmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
2. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2 ndEdition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and

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M. Tech I Year I semester

Response", William Pollock Publisher, 2013.

Course Outcomes(CO):

On completion of this course, student will be able to:

CO1: Identify and utilize different forms of cryptography techniques.

CO2: Incorporate authentication and security in the network applications.

CO3: Analyze symmetric key cryptographic algorithms and evaluate their strengths and weaknesses using cryptanalysis techniques.

CO4: Describe the principles of public-key cryptography for secure communication.

CO5: Distinguish among different types of threats to the system and handle the same.

CO6: Design Secure communication systems.

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M. Tech I Year I semester

CMOS DIGITAL IC DESIGN LAB

Course Code	L:T:P	Credits	Exam. Marks	Exam Duration	Course Type
25MEV01P	0:0:4	2	CIE:30 SEE:70	3 Hours	PC

Syllabus

LIST OF EXPERIMENTS:

The students are required to design and implement the Circuit and Layout of any TEN Experiments using CMOS 130nm Technology.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter
11. Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

Lab Requirements:

Software: Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software
Hardware: Personal Computer with necessary peripherals, configuration and operating System.

Course Outcomes:

After the completion of the course students will be able to:

CO1: Explain the VLSI Design Methodologies using any VLSI design tool.
CO2: Grasp the significance of various design logic Circuits in full-custom IC Design.
CO3: Explain the Physical Verification in Layout Extraction.
CO4: Fully appreciate the design and analyze of CMOS Digital Circuits.
CO5: Grasp the Significance of Pre-Layout Simulation.
CO6: Grasp the Significance of Post-Layout Simulation.

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M. Tech I Year I semester

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS LAB

Course Code	L:T:P	Credits	Exam. Marks	Exam Duration	Course Type
25MEV02P	0:0:4	2	CIE:30 SEE:70	3 Hours	PC

Syllabus

LIST OF EXPERIMENTS:

Part A

Experiments to be carried out on Cortex-Mx development boards and using GNU toolchain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED once every five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

Part B

Experiments to be carried out on DSP C6713 evaluation kits and using Code Composer Studio (CCS)

12. To develop an assembly code and C code to compute Euclidian distance between any two points
13. To develop assembly code and study the impact of parallel, serial and mixed execution
14. To develop assembly and C code for implementation of convolution operation
15. To design and implement filters in C to enhance the features of given input sequence/signa

Software Requirements: Keil for ARM, Code Composer Studio
Hardware Requirements: ARM Cortex Mx Development Boards, TI TMS C6713 evaluation kit

Course Outcomes:

After the completion of the course students will be able to:

CO1: Install, configure and utilize tool sets for developing applications based on ARM processor core.
CO2: Design and develop theARM7 based embedded systems for various applications.
CO3: Develop application programs on ARM and DSP development boards in assembly Language.
CO4: Develop application programs on ARM and DSP development boards in C Language.
CO5: Design and Implement the digital filters on DSP6713 processor.
CO6: Analyze the hardware and software interaction and integration.

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RESEARCH METHODOLOGY AND IPR					
Course Code	**L:T:P:S**	**Credits**	**Exam marks**	**Exam Duration**	**Course Type**
25MMC01	**2:0:0:0**	**2**	**CIE:30 SEE:70**	**3 Hours**	**MC**

Course Objectives:

- To understand the research design process and data collection methods.
- To develop skills in data analysis and reporting.
- To familiarize students with intellectual property rights (IPR) and patents.
- To apply research skills in real-world contexts.

Syllabus		**Total Hours: 45**
Unit-I	**Fundamentals of Research Methodology**	**9 Hrs**
Overview of research process and design - Types of Research - Approaches to Research (Qualitative vs Quantitative) - Observation studies, Experiments and Surveys - Use of Secondary and exploratory data to answer the research question - Importance of Reasoning in Research and Research ethics - Documentation Styles (APA/IEEE etc.) - Plagiarism and its consequences		
Unit-II	**Data Collection and Sources**	**9 Hrs**
Importance of Data Collection - Types of Data - Data Collection Methods - Data Sources - primary, secondary and Big Data sources - Data Quality & Ethics - Tools and Technology for Data Collection		
Unit –III	**Data Analysis and Reporting**	**9 Hrs**
Overview of Multivariate analysis - Experimental research, cause-effect relationship, and development of hypotheses- Measurement systems analysis, error propagation, and validity of experiments - Guidelines for writing abstracts, introductions, methodologies, results, and discussions - Writing Research Papers & proposals		
Unit –IV	**Understanding Intellectual Property Rights**	**9 Hrs**
Intellectual Property – The concept of IPR, Evolution and development of concept of IPR, IPR development process, Trade secrets, utility Models, IPR & Bio diversity, Role of WIPO and WTO in IPR establishments, Right of Property, Common rules of IPR practices, Types and Features of IPR Agreement, Trademark, Functions of UNESCO in IPR maintenance.		
Unit –V	**Patents**	**9 Hrs**
Patents – objectives and benefits of patent, Concept, features of patent, Inventive step, Specification - Types of patent application, process E-filling, Examination of patent, Grant of patent, Revocation, Equitable Assignments, Licenses, Licensing of related patents, patent agents, Registration of patent agents		

Textbooks:

1. Stuart Melville and Wayne Goddard, Research Methodology: An introduction for Science & Engineering students, Juta and Company Ltd, 2004.
2. Catherine J. Holland, Intellectual property: Patents, Trademarks, Copyrights, Trade Secrets, Entrepreneur Press, 2007.

Reference Books:

1. Cooper Donald R, Schindler Pamela S and Sharma JK, "Business Research Methods", Tata McGraw Hill Education 11e (2012).
2. Ranjit Kumar , Research Methodology: A Step-by-Step Guide for Beginners. . David Hunt, Long

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Nguyen, Matthew Rodgers, "Patent searching: tools & techniques", Wiley, 2007.
3. Deborah E. Bouchoux , Intellectual Property: The Law of Trademarks, Copyrights, Patents, and Trade Secrets, 6th Edition, Cengage 2024.
4. Wayne C. Booth, Gregory G. Colomb, Joseph M. Williams, The Craft of Research, 5th Edition, University of Chicago Press, 2024.

Online Resources (Free & Authentic)

- **Coursera / edX** – Research Methodology and Data Analysis courses
- **Springer Link & ScienceDirect** – Latest journals on research design and statistics
- **Google Scholar** – Free access to research papers
- **NCBI Bookshelf** – Open-access research methodology resources
- **Khan Academy (Statistics & Probability)** – For fundamentals of hypothesis testing, regression, and ANOVA.

Course Outcomes(CO):

On completion of this course, student will be able to:

CO1: Recall key concepts and terminology related to research design, data collection, and intellectual property rights.

CO2: Explain the importance of research design and data analysis in research studies, and describe the concept of intellectual property rights.

CO3: Design a research study, including data collection and analysis methods, and apply intellectual property rights principles to protect research findings.

CO4: Analyze research studies to identify strengths and limitations, and evaluate the effectiveness of data collection and analysis methods.

CO5: Assess the impact of intellectual property rights on research and innovation, and evaluate the effectiveness of research designs and methods.

CO6: Develop a comprehensive research plan, including a detailed research design, data collection and analysis methods, and a plan for protecting intellectual property.

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RTL SYNTHESIS, SIMULATION AND VERIFICATION

Course Code	L:T:P	Credits	Exam. Marks	Exam Duration	Course Type
25MSE01	0:1:2	2	CIE:30 SEE:70	3 Hours	SE

Syllabus

Module 1 – Introduction to RTL Design

- RTL design flow: Specification → RTL coding → Synthesis → Simulation → Verification.
- HDL coding styles for synthesis (System Verilog/VHDL basics).
- Lab:
  1. Write synthesizable Verilog /System Verilog code for:
     a) Half Adder, Full Adder
     b) 4-bit Ripple Carry Adder
     c) 4-bit Synchronous Counter (Up/Down)
  2. FSM Design: Sequence Detector (e.g., detect "1011").

Module 2 – RTL Synthesis

- Synthesis concepts: mapping RTL to gate-level netlist.
- Constraints: clock, area, power.
- Lab:
  1. Synthesize combinational and sequential circuits (Adder, Counter, FSM) using EDA tool
  2. Generate gate-level netlist and analyze area, delay, power reports.
  3. Apply constraints (clock, timing) and observe impact on synthesis results.

Module 3 – Simulation

- Functional vs. Timing simulation.
- Test bench creation, waveforms, debugging.
- Lab: Run simulations
  1. Develop test benches for:
     a) 4-bit ALU (add, sub, AND, OR).
     b) Universal Shift Register.
  2. Perform functional simulation using EDA tools
  3. Perform post-synthesis (timing) simulation and compare results with functional simulation.

Module 4 – Verification

- Verification basics: functional verification, assertion-based verification.
- Introduction to UVM/OVM concepts.
- Lab: Writing simple verification test benches.
  1. Write self-checking test benches for combinational and sequential circuits.
  2. Use assertion-based verification (System Verilog Assertions – SVA) for protocol checks (e.g., handshaking signals).
  3. Coverage-driven verification experiment: Create random test cases for FIFO/Memory.

Module 5 – Case Study & Mini Project

- Design, synthesize, and verify a digital subsystem (e.g., ALU, UART, FIFO).
- End-to-end RTL → Synthesis → Simulation → Verification flow.
- Lab: Design, synthesize, simulate, and verify a **digital subsystem** such as:

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1. UART Transmitter/Receiver
2. Simple CPU Core Module (Instruction Decoder + ALU + Register File)
3. FIFO Buffer with full/empty flags

Textbooks / References

1. Samir Palnitkar – *Verilog HDL: A Guide to Digital Design and Synthesis*.
2. Michael Ciletti – *Advanced Digital Design with the Verilog HDL*.
3. Chris Spear & Greg Tumbush – *SystemVerilog for Verification*.
4. David Rich – *Design and Verification with SystemVerilog*.

Course Outcomes:

After the completion of the course students will be able to:

CO1: Demonstrate the process steps required for simulation /synthesis.

CO2: Design and simulate various combinational circuits using HDL.

CO3: Design and simulate various sequential circuits using HDL.

CO4: Develop an RTL code for various real time applications.

CO5: Synthesize / Simulate an RTL code for several digital designs

CO6: Build and verify various digital circuits.

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M. Tech I Year I semester

IOT AND RTOS FOR EMBEDDED APPLICATIONS

Course Code	L:T:P	Credits	Exam. Marks	Exam Duration	Course Type
25MSE02	0:1:2	2	CIE:30 SEE:70	3 Hours	SE

Syllabus

Module 1: IoT Hardware & Sensors
Introduction to IoT and embedded devices, Raspberry Pi and BeagleBone Black: Architecture, GPIO, SPI, I2C interfaces, Basics of interfacing digital and analog sensors/actuators, Interfacing LEDs, Buzzer, Push Button, IR, and LDR sensors.

Experiments:
1. Setup Raspberry Pi, install OS and necessary software, test basic connectivity.
2. Interface LED and Buzzer; write Python program to blink LED periodically.
3. Interface Push Button or IR/LDR sensor; program to control LED based on input.

Module 2: IoT Data Collection & Cloud Integration
Reading environmental sensors (temperature, humidity), IoT communication protocols: MQTT, HTTP, REST APIs, Cloud integration using Thingspeak, MQTT brokers.

Experiments:
1. Interface DHT11 sensor with Raspberry Pi; display temperature and humidity readings.
2. Upload sensor data to Thingspeak cloud and retrieve for visualization.
3. Publish and subscribe sensor data using MQTT on BeagleBone Black.

Module 3: Real-Time Operating Systems (RTOS) Fundamentals
Differences between Traditional OS and RTOS, Hard vs. Soft real-time systems; timing constraints and task scheduling, and multitasking concepts, Scheduling algorithms.

Experiments:
1. Introduction to VxWorks RTOS: kernel, task assignment, and multitasking basics.
2. Timer programming in VxWorks.
3. Create tasks and implement Round Robin scheduling.

Module 4: Inter-Process Communication (IPC) in RTOS
Task synchronization and communication, Semaphores: Binary and Counting, Message queues and mailboxes, Mutexes and critical sections.

Experiments:
1. Task communication using message queues in VxWorks.
2. Synchronize tasks using semaphores.
3. Implement IPC using mailboxes for data exchange between tasks.

Module 5: IoT Application Design
Designing integrated IoT solutions combining sensors, actuators, cloud, and RTOS tasks

Experiments (Choose one):
1. Design a weather monitoring system with real-time cloud data upload.

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2. Smart home automation: Control lights/fans based on sensor inputs.
3. IoT-based vending machine prototype using VxWorks and sensors.

Suggested Reading:

1. Arshdeep Bahga and Vijay Madisetti, *Internet of Things: A Hands-on Approach*, Universities Press, 2015.
2. Jane W.S. Liu, *Real-Time Systems*, Pearson Education, Asia, 2018.
3. Wind River Systems Inc., *VxWorks Programmers Guide*, 2019.
4. C. M. Krishna and G. Shin, *Real-Time Systems*, McGraw-Hill, 2015.
5. Practical Python Programming for IoT: Build advanced IoT projects using Raspberry Pi, MQTT, RESTful APIs, WebSockets, and Python 3, 2020

Course Outcomes:

After the completion of the course students will be able to:

CO1: Demonstrate interfacing of sensors and actuators with IoT devices.

CO2: Acquire and integrate sensor data with cloud platforms using IoT protocols.

CO3: Apply RTOS concepts for multitasking.

CO4: Apply RTOS concepts for task scheduling.

CO5: Implement inter-process communication techniques in RTOS

CO6: Design and develop IoT applications using embedded systems and RTOS.

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TECHNICAL RESEARCH PAPER WRITING

Course Code	L:T:P:S	Credits	Exam marks	Exam Duration	Course Type
25MAC01	2:0:0:0	-	CIE:30	3 Hours	AC-I

Course Objectives:

- Understand the essentials of writing skills and their level of readability
- Learn about what to write in each section
- Ensure qualitative presentation with linguistic accuracy

Syllabus	Total Hours: 45
Unit-I	**9 Hrs**
Overview of a Research Paper- Planning and Preparation- Word Order- Useful Phrases - Breaking up Long Sentences-Structuring Paragraphs and Sentences-Being Concise and Removing Redundancy -Avoiding Ambiguity	
Unit-II	**9 Hrs**
Essential Components of a Research Paper- Abstracts- Building Hypothesis-Research Problem - Highlight Findings- Hedging and Criticizing, Paraphrasing and Plagiarism, Cauterization	
Unit –III	**9 Hrs**
Introducing Review of the Literature – Methodology - Analysis of the Data-Findings – Discussion Conclusions-Recommendations.	
Unit –IV	**9 Hrs**
Key skills needed for writing a Title, Abstract, and Introduction	
Unit –V	**9 Hrs**
Appropriate language to formulate Methodology, incorporate Results, put forth Arguments and draw Conclusions	

Suggested Reading:

1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books) Model Curriculum of Engineering & Technology PG Courses [Volume-I]
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman's book
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

Course Outcomes(CO):

On completion of this course, student will be able to:

CO1: Understand the significance of writing skills and the level of readability.
CO2: Analyze and write title, abstract, different sections in research paper.
CO3: Develop the skills needed while writing a research paper.
CO4: Demonstrate the ability to write effective titles, abstracts, and introductions that accurately reflect the content and scope of the research paper.
CO5: Use appropriate academic language to describe methodology, present results, construct arguments, and draw meaningful conclusions.
CO6: Compose a well-organized and coherent research paper by integrating structural, linguistic, and ethical principles of academic writing.

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M. Tech I Year I semester

DISASTER MANAGEMENT

Course Code	L:T:P:S	Credits	Exam marks	Exam Duration	Course Type
25MAC02	2:0:0:0	-	CIE:30	3 Hours	AC-I

Syllabus — **Total Hours: 45**

Unit-I — **9 Hrs**

Introduction: Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster; Natural and Manmade Disasters: Difference, Nature, Types and Magnitude. Disaster Prone Areas in India: Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics

Unit-II — **9 Hrs**

Repercussions of Disasters and Hazards: Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones, Tsunamis, Floods, Droughts and Famines, Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

Unit –III — **9 Hrs**

Disaster Preparedness and Management: Preparedness: Monitoring of Phenomena Triggering A Disaster or Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness

Unit –IV — **9 Hrs**

Risk Assessment Disaster Risk: Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participation in Risk Assessment. Strategies for Survival.

Unit –V — **9 Hrs**

Disaster Mitigation: Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends In Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India

Suggested Reading:

1. R. Nishith, Singh A K, "Disaster Management in India: Perspectives, issues and strategies "'New Royal book Company. Sahni, Pardeep Et.Al. (Eds.),
2. "Disaster Mitigation Experiences And Reflections", Prentice Hall Of India, New Delhi.
3. Goel S. L., Disaster Administration And Management Text And Case Studies", Deep & Deep Publication Pvt. Ltd., New Delhi

Course Outcomes(CO):

On completion of this course, student will be able to:

CO1: Learn to demonstrate critical understanding of key concepts in disaster risk reduction and humanitarian response.

CO2: Critically evaluate disaster risk reduction and humanitarian response policy and practice from Multiple perspectives.

CO3: Develop an understanding of standards of humanitarian response and practical relevance inspecific types of disasters and conflict situations

CO4: Critically understand the strengths and weaknesses of disaster management approaches, planning and programming in different countries, particularly their home country or the countries they work in.

CO5: Demonstrate knowledge of structural and non-structural disaster mitigation strategies

CO6: Examine the emerging trends and mitigation programs.

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ESSENCE OF INDIAN TRADITIONAL KNOWLEDGE					
Course Code	**L:T:P:S**	**Credits**	**Exam marks**	**Exam Duration**	**Course Type**
25MAC03	**2:0:0:0**	**-**	**CIE:30**	**3 Hours**	**AC-I**

Course Objectives:

- To facilitate the students with the concepts of Indian traditional knowledge and to make them understand the importance of roots of knowledge system
- To make them understand the need for protecting traditional knowledge and its significance in the global economy
- To make them understand the legal frame work and policies related to traditional knowledge protection
- To enable them to understand the relationship between traditional knowledge and intellectual property rights
- To make them explore the applications of traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology

Syllabus	**Total Hours: 45**
Unit-I	**9 Hrs**

Introduction to traditional knowledge - Definition, Nature and characteristics, scope and importance - Kinds of traditional knowledge - Physical and social contexts in which traditional knowledge develop - Historical impact of social change on traditional knowledge systems - Indigenous Knowledge (IK) – Characteristics - traditional knowledge vis-à-vis indigenous knowledge -Traditional knowledge Vs western knowledge, traditional knowledge vis-à-vis formal knowledge

Learning Outcomes:

At the end of the unit the student will able to:

- Understand the concept of traditional knowledge.
- Contrast and compare characteristics, importance& kinds of traditional knowledge.
- Analyze physical and social contexts of traditional knowledge.
- Evaluate social change on traditional knowledge.

Unit-II	**9 Hrs**

Protection of traditional knowledge- Need for protecting traditional knowledge - Significance of TK Protection - Value of TK in global economy - Role of Government to harness TK.

Learning Outcomes:

At the end of the unit the student will able to:

- Know the need of protecting traditional knowledge.
- Apply significance of TK protection.
- Analyze the value of TK in global economy.
- Evaluate role of government

Unit -III	**9 Hrs**

Legal frame work and TK - A)The Scheduled Tribes and Other Traditional Forest Dwellers (Recognition of Forest Rights) Act, 2006 - Plant Varieties Protection and Farmer's Rights Act, 2001 (PPVFR Act) – B)The Biological Diversity Act 2002 and Rules 2004 - the protection of traditional knowledge bill, 2016 - Geographical Indicators Act 2003.

Learning Outcomes:

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At the end of the unit the student will able to:

- Understand legal frame work of TK.
- Contrast and compare the ST and other traditional forest dwellers
- Analyze plant variant protections
- Understand the rights of farmers forest dwellers

Unit -IV	**9 Hrs**

Traditional knowledge and Intellectual property - Systems of traditional knowledge protection - Legal concepts for the protection of traditional knowledge - Certain non-IPR mechanisms of traditional knowledge protection - Patents and traditional knowledge - Strategies to increase protection of traditional knowledge - Global legal FORA for increasing protection of Indian Traditional Knowledge.

Learning Outcomes:

At the end of the unit the student will able to:

- Understand TK and IPR
- Apply systems of TK protection.
- Analyze legal concepts for the protection of TK.
- Evaluate strategies to increase the protection of TK.

Unit -V	**9 Hrs**

Traditional knowledge in different sectors - Traditional knowledge and Engineering - Traditional medicine system - TK and Biotechnology - TK in Agriculture - Traditional societies depend on it for their food and healthcare needs - Importance of conservation and sustainable development of environment - Management of biodiversity, Food security of the country and protection of TK

Learning Outcomes:

At the end of the unit the student will be able to:

- Know TK in different sectors.
- Apply TK in Engineering.
- Analyze TK in various sectors.
- Evaluate food security and protection of TK in the country.

Prescribed Books:

1. Mahadevan, B., Bhat Vinayak Rajat, Nagendra Pavana R.N. Introduction to Indian Knowledge System: Concepts and Applications, PHI Learning Pvt.Ltd. Delhi, 2022.
2. 2.Basanta Kumar Mohanta and Vipin Kumar Singh,Traditional Knowledge System and Technology in India, PratibhaPrakashan 2012.

Reference Books:

1. Pride of India: A Glimpse into India's Scientific Heritage, Samskrita Bharati, New Delhi.
2. Kak, S.C. "On Astronomy in Ancient India", Indian Journal of History of Science, 22(3), 1987
3. Subbarayappa, B.V. and Sarma, K.V. Indian Astronomy: A Source Book, Nehru Centre, Mumbai, 1985.
4. Bag, A.K. History of Technology in India, Vol. I, Indian National Science Academy, New Delhi, 1997.
5. Acarya, P.K. Indian Architecture, Munshiram Manoharlal Publishers, New Delhi, 1996.
6. Banerjea, P. Public Administration in Ancient India, Macmillan, London, 1961.
7. Kapoor Kapil, Singh Avadhesh,Indian Knowledge Systems Vol – I & II, Indian Institute of Advanced

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M. Tech I Year I semester

Study, Shimla, H.P., 2022

Course Outcomes(CO):

On completion of this course, student will be able to:

CO1: Define and explain the concept of traditional knowledge, its nature, characteristics, and scope.

CO2: Understand the need for protecting traditional knowledge and its significance in the global economy.

CO3: Explain the legal framework and policies related to traditional knowledge protection.

CO4: Apply traditional knowledge in different sectors, such as engineering, medicine, agriculture, and biotechnology.

CO5: Analyze the importance of traditional knowledge in various contexts, including its historical impact and social change.

CO6: Analyze the relationship between traditional knowledge and intellectual property rights, including patents and non-IPR mechanisms.