GEETHANJALI INSTITUTE OF SCIENCE & TECHNOLOGY

(Unit of USHODAYA EDUCATIONAL SOCIETY, Nellore)

(Approved by AICTE, New Delhi & Permanently Affiliated to JNTUA, Anantapur)

An ISO 9001 : 2015 Certified Institution - Recognised U/s. 2(f) & 12(B) of UGC Act 1956

3rd Mile, Nellore - Bombay Highway, Gangavaram (V), Kovur (M), S.P.S.R. Nellore Dt, Andhra Pradesh - India, 524 137

JNTUA College Code : 2U

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III B.TECH II SEM MID-II EXAMINATIONS

DESCRIPTIVE QUESTION PAPER

Name of the subject	VLSI DESIGN	Duration	90 MINUTES
Date of Exam	17.08.2021 AN	BRANCH	ECE
H T NO.		Sign of Invigilator	

ANSWER ANY THREE QUESTIONS — **MAX 30 M**

S.No	UNIT	Blooms Taxonomy	CO	QUESTION DESCRIPTION	MARKS
1	III	Understand	CO4	2. Explain with suitable examples how to design the layout of a gate to maximize performance and minimize area.	10
2	IV	Understand	CO5	5. Explain about any one multiplier architecture in VLSI design. What are the challenging issues to be considered for the same.	10
3	IV	Analyse	CO5	4. Illustrate with neat architecture diagram and explain about various functional blocks of FPGA.	10
4	V	Understand	CO6	7. Explain about different fault models in VLSI testing with examples.	10
5	V	Analyse	CO6	10a. Write a short note on circuit synthesis.	4
				10b. Give comparison of design capture tools and design verification tools.	6

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III B.TECH II SEM MID-II EXAMINATIONS

OBJECTIVE QUESTION PAPER

Name of the subject	VLSI DESIGN	Duration	20 MINUTES
Date of Exam	17.08.2021 AN	BRANCH	ECE
H T NO.		Sign of Invigilator	

ANSWER ALL QUESTIONS — 10 M

S.No	UNIT	QUESTION DESCRIPTION	ANSWER
1	V	In which mode, storage elements are used independently? A. test 1 mode B. test 2 mode C. normal mode D. final mode	
2	IV	Approach used for design process are A. circuit symbols B. all of the mentioned C. logic symbols D. stick diagrams	
3	V	Delay fault is considered as: A. Physical defect B. Electrical fault C. Logical fault D. None of the Mentioned	
4	V	ATPG stands for: A. Attenuated Transverse wave Pattern Generation B. Aligned Test Parity Generator C. None of the mentioned D. Automatic Test Pattern Generator	
5	IV	Multipliers are built using A. multiplexers B. binary adders C. binary subtractors D. dividers	
6	IV	VLSI design is done in ____ approach A. bottom-up B. semi random C. random D. top-down	
7	III	Features of switch logic approach A. occupies more area B. ow power dissipation C. no undesirable threshold voltage D. all of the mentioned	
8	III	Power dissipation in switch logic is A. high B. less C. more D. very less	
9	IV	The shifter must be connected to A. 2-shift data line B. 2-shift control line C. 4-shift data line D. 4-shift control line	
10	IV	Which multiplier is very well suited for twos complement numbers? A. baugh-wooley algorithm B. modified booth encoding C. wallace trees D. dadda multipliers	
11	V	_____ of the area is dedicated for testability A. 10% B. 20% C. 30% D. 25%	
12	IV	In the adder, sum is stored in A. cascade B. parallel C. registers D. series	
13	III	Gate logic is also called as A. complementary logic B. transistor logic C. restoring logic D. switch logic	
14	III	The subsystem of the circuits should have _____ interdependence A. maximum B. no C. more D. minimum	
15	V	The circuit should be tested at A. transistor level B. chip level C. design level D. switch level	
16	III	Switch logic is based on A. pass transistors B. design rules C. pass transistors and transmission gates D. transmission gates	
17	IV	To minimize the design effort, regularity should be A. very high B. very low C. high D. low	
18	III	In CMOS NAND gate, p transistors are connected in A. series B. random C. cascade D. parallel	
19	V	Built-in self test aims to A. reduce volume of test data B. reduce test pattern generation cost C. all of the mentioned D. reduce test time	
20	III	As the number of inputs increases, the NAND gate delay A. increases B. exponentially decreases C. decreases D. does not vary	