

Faculty Contributions:**Publications:**

- Mrs. K. Radhika published a paper on Satellite Image Classification Based On Ensemble Subspace Discriminant Method Using Random Subspace Algorithm in Helix 2719-2725 Vol. 08 / December 2017.
- Mrs. K. Radhika presented a paper “Satellite Image Classification based on Ensemble Subspace Discriminant method using Random Subspace Algorithm”, in International Conference on Emerging Trends in Engineering (**ICACS-2017**), 21st October 2017, at SVCE, Tirupati, Andhra Pradesh.
- Mrs. K. Radhika presented a paper “A Random Subspace based classification for change detection of satellite images”, in International Conference on Emerging Trends in Engineering (ICACS-2017), 21st October 2017, at SVCE, Tirupati, Andhra Pradesh.

Workshop/ Fdp Attended:

- Mr. M. Sivakrishna have attended a Two Day Workshop on Introduction to Machine Learning conducted by GIST & IIT, Kharagpur during 16th December to 17th December 2017.
- Ms .M. Suhasini have attended a Two Day Workshop on Introduction to Machine Learning conducted by GIST & IIT, Kharagpur during 16th December to 17th December 2017.
- Mr.P.V.Krishna Rao have attended a Two Day Workshop on Introduction to Machine Learning conducted by GIST & IIT, Kharagpur during 16th December to 17th December 2017.
- Mr. Naveen Kolla, Attended “Pedagogy for Online and Blended Teaching - Learning Process” conducted by IIT BOMBAY, under AICTE and PMMMNMTT, MHRD Nellore from 14-9-2017 to 12-10-2017.
- Mr. M.Sivakrishna, Attended “Pedagogy for Online and Blended Teaching - Learning Process” conducted by IIT BOMBAY, under AICTE and PMMMNMTT, MHRD Nellore from 14-9-2017 to 12-10-2017.
- Mr. S.Sreenivasulu, Attended “Pedagogy for Online and Blended Teaching - Learning Process” conducted by IIT BOMBAY, under AICTE and PMMMNMTT, MHRD Nellore from 14-9-2017 to 12-10-2017.
- Mrs. M.Suhasini, Attended “Pedagogy for Online and Blended Teaching - Learning Process” conducted by IIT BOMBAY, under AICTE and PMMMNMTT, MHRD Nellore from 14-9-2017 to 12-10-2017.

Events Organized:**GUEST LECTURE ON “CAREER OPPORTUNITIES FOR ENGINEERING ASPIRANTS”:**

A Guest lecture on “Career Opportunities for Engineering Aspirants” was Organized by Department of ECE, GIST by the Strategic Marketing, Ace Engineering Academy, Hyderabad on 26-10-2017. He addressed II B-Tech ECE Students in New Seminar Hall More than 200 students get the benefit of this lecture in new seminar hall.

**PARENTS MEETING:**

A parents meeting was held for the parents and students of II, III, IV ECE branch on 29.10.2017, i.e. Sunday with the objective of appraising the parents of the academic progress of their wards and addressing issues if, any concerning the academic administration of the campus. Over 450 parents and students actively involved themselves in the meet and several parents interacted with the principal regarding a number of issues related to academic performance of their wards.

**INDUSTRIAL VISIT TO NARL:**

NARL is an autonomous research laboratory fully funded by the Department of Space, Government of India and involved in carrying out fundamental and applied research in Atmospheric and Space Sciences. NARL has now become one of the prime centers for atmospheric research in the country and operates a state-of-the-art MST radar. Industrial visit was carried out at NARL Gadanki on 13th October 2017 for III year and IV year students.

**Student Achievements:****Won Prizes/Internships/Project Expo:**

- Ms.V.Adbhuta Teja of III B.Tech,ECE won 2nd place in “Extempore talk” in World Space Week 2017 Celebrations conducted by SDSC SHAR, ISRO, Sriharikota during 8th to 10th October 2017 held at Geethanjali Institute of Science & Technology, Nellore .

- Ms.Shaik. Arshiya Tabassum of III ECE secured college First Place in TI Online National Webinar Contest on Linear Integrated Circuits conducted by Texas Instruments,Bangalore held on 23rd October 2017 at Geethanjali Ins Of Sci & Tech,Nellore.
- Mr.Gali Bhanu Teja of III ECE secured college second Place in TI Online National Webinar Contest on Linear Integrated Circuits conducted by Texas Instruments,Bangalore on 23rd October 2017 at Geethanjali Ins Of Sci & Tech,Nellore.
- Ms Gundala Divya Reddy of III ECE secured college Third Place in TI Online National Webinar Contest on Linear Integrated Circuits conducted by Texas Instruments,Bangalore on 23rd October 2017 at Geethanjali Ins Of Sci & Tech,Nellore.
- Ms.Shaik Rahilabhanu of IV ECE secured college fourth Place in TI Online National Webinar Contest on Linear Integrated Circuits conducted by Texas Instruments,Bangalore on 23rd October 2017 at Geethanjali Ins Of Sci & Tech,Nellore.
- Mr.Mavuduru Sri Hari, of III ECE ,Ms.Nimmala Anitha, Ms. Gundala Veena Reddy, MsVavveti Sireesha of IV ECE secured college Fourth Place in TI Online National Webinar Contest on Embedded system Design Using MSP 430 conducted by Texas Instruments Bangalore on 27th October 2017 at Geethanjali Ins Of Sci & Tech,Nellore .
- The project titled “DESIGN AND DEVELOPMENT OF DATALOGGER FOR LIVE TRACKING OF VEHICLES “designed by Ms.SD Mohana Priya of IV ECE, Ms.G Divya Reddy, Ms.Shaik Arshiya Tabassum of III ECE is shortlisted for State Level Project Exhibition to held in Amaravathi ,Vijayawada.
- The project titled DROT designed by Mr.K Pradhyunma Kumar, Mr.Vamsi M, Mr. P Sreenivasulu of IV ECE is shortlisted for State Level Project Exhibition to held in Amaravathi ,Vijayawada.
- The project titled IOT BASED IRRIGATION SYSTEM designed by Ms,Shaik Arifa, Ms. R Sri Lakshmi of IV ECE is shortlisted for State Level Project Exhibition to held in Amaravathi , Vijayawada.
- The project titled DROT designed by Mr.K Pradhyunma Kumar, Mr.Vamsi M, Mr. P Sreenivasulu of IV ECE is shortlisted for National Level Project Exhibition Rapid Prototyping Camp , at Intel Higher Education 2017 on Cyber Physical Systems at SJB Institute of Technology, Bangalore.
- Mr.G.Yaswanth Reddy ,IV B.Tech ECE secured Campus Ambassador Internship at Entrepreneurship Cell,Delhi Technological University through INTERNSHALA on 27th October 2017.
- Mr.M.Vamsi and Mr.P.Sreenivasulu of IV B.Tech,ECE completed two months training & internship in “Angular JS “ from 5th November 2017 to 6th January 2018 in ACE WEB ACADEMY,Hyderabad.
- Mr.K.Pradhyunma Kumar of IV B.Tech,ECE had undergone a six week online winter training on WEB DEVELOPMENT from 6th December 2017 to 16th January 2018 through Internshala Trainings
- Mr. RVS. Narayana Kumar and Mr.G.Ravi Teja of III B.Tech,ECE successfully completed “Mini Project on “Implementation of Digital Filters on SHARC Processors using C “from 15th December 2017 to 06th January 2018 at Directorate of Navigation & Embedded Computers, Research Centre, Imarat,(DRDO),Hyderabad.

Editorial Board: Editors: 1. Mr.M. Sivakrishna, 2. Mrs.C.Durga Tejaswi,

Student Members: 1.Shaik Mahammad (III ECE), 2. Thurimerla Srikanth (III ECE)

3. .M. Sudivya (II ECE), 4. N. Saiteja (II ECE),



GEETHANJALI INSTITUTE OF SCIENCE AND TECHNOLOGY
(Approved by AICTE, New Delhi & Affiliated to JNTU, Anantapur)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

NEWS LETTER

ABSOLUTE ELECTRONICS

“Key to Success”

Vision

To become a reputed learning centre producing competent professionals.

Mission

- Provide Quality education through interactive teaching-learning practices.
- Establish Technology-enabled environment for core competencies including robotics.
- Arrange Industry-Interaction to hone professional skills.
- Organize activities to foster social skills and ethical values.

VLSI TECHNOLOGY

VLSI Technology, Inc., was a company that designed and manufactured custom and semi-custom integrated circuits (ICs). The company was based in Silicon Valley, with headquarters at 1109 McKay Drive in San Jose. Along with LSI Logic, VLSI Technology defined the leading edge of the application-specific integrated circuit (ASIC) business, which accelerated the push of powerful embedded systems into affordable products.

VLSI chiefly comprises of Front End Design and Back End design these days. While front end design includes digital design using HDL, design verification through simulation and other verification techniques, the design from gates and design for testability, backend design comprises of CMOS library design and its characterization. It also covers the physical design and fault simulation.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

- Apply Engineering concepts to solve Electronics and Communication Engineering problems of social relevance.
- Design and develop Electronic devices and Systems for Industry or pursue research.
- Demonstrate competencies through continuous learning and adapt to multi-disciplinary environment.
- Practice professional values and contribute to the societal needs.

PROGRAM SPECIFIC OUTCOMES (PSOs)

- Professional Skills: Apply principles of Analog and Digital Electronics, Communication Systems, Image processing, VLSI and Embedded Systems to solve diverse problems.
- Software Knowledge: Develop solutions for complex engineering problems of social relevance by employing Xilinx, CC Studio, Micro Wind, Keil, NG Spice, Scilab tools.