Faculty Achievements:

- Mrs.G.Kameswari Assoc.Prof had participated in "Pedagogy workshop for Effective Use of ICT in Engineering Education" from 5th Jan to 31st Jan, 2015 by IIT BOMBAY.
- Mr.P.Raghava Reddy Assoc.Prof, had participated in "Pedagogy workshop for Effective Use of ICT in Engineering Education" from 5th Jan to 31st Jan, 2015 by IIT BOMBAY.
- Mr.V.Bhaskar Rao Assoc.Prof had participated in "Pedagogy workshop for Effective Use of ICT in Engineering Education" from 5th Jan to 31st Jan, 2015 by IIT BOMBAY.
- Mr.T.V.Sridhar Assoc.Prof had participated in "Pedagogy workshop for Effective Use of ICT in Engineering Education" from 5th Jan to 31st Jan, 2015 by IIT BOMBAY.
- Mr.G.Kiran Kumar Asst.Prof had participated in "Pedagogy workshop for Effective Use of ICT in Engineering Education" from 5th Jan to 31st Jan, 2015 by IIT BOMBAY.
- Mrs.D.Nagajyothi Asst.Prof had participated in "Pedagogy workshop for Effective Use of ICT in Engineering Education" from 5th Jan to 31st Jan, 2015 by IIT BOMBAY.
- Mr.K.Prabhakar Reddy Asst.Prof , Mr.T.Chiranjeevi Asst.Prof, Ms.G.Meenakshi Asst.Prof, and Ms.Masthan- E-Shahina Shaik Asst.Prof had participated in "*Pedagogy workshop for Effective Use of ICT in Engineering Education*" from 5th Jan to 31st Jan, 2015 by *IIT BOMBAY*.
- Mr.K.Prabhakar Reddy Asst.Prof had participated in "Pedagogy workshop for Effective Use of ICT in Engineering Education" from 5th Jan to 31st Jan, 2015 by IIT BOMBAY.
- Mr.T.Chiranjeevi Asst.Prof, Ms.G.Meenakshi Asst.Prof, and Ms.Masthan-E-Shahina Shaik Asst.Prof had participated in "*Pedagogy workshop for Effective Use of ICT in Engineering Education*" from 5th Jan to 31st Jan, 2015 by *IIT BOMBAY*.
- Ms.G.Meenakshi Asst.Prof, and Ms.Masthan- E-Shahina Shaik Asst.Prof had participated in "Pedagogy workshop for Effective Use of ICT in Engineering Education" from 5th Jan to 31st Jan, 2015 by IIT BOMBAY.

Student Achievements:

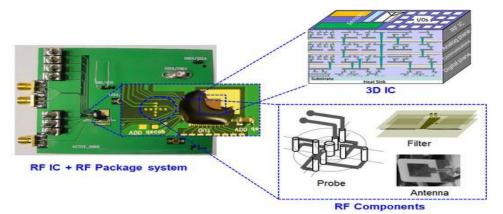
- N.Sukanya had participated and secured Ist prize in the event of paper presentation at the National Level Technical Symposium organized by Jagan's College of Engineering on 14th march, 2015.
- T.V.Supriya(122U1A04F8) had participated and secured Ist prize in the event of paper presentation at the National Level Technical Symposium organized by Jagan's College of Engineering on 14th march, 2015.
- M.Sravanthi(122U1A0482) had participated in the event of paper presentation at the National Level Technical Symposium organized by Geethanjali Institute of science and Technology,Nellore on 19th march, 2015.
- M. Jaswanthi(122U1A0481) had participated in the event of paper presentation at the National Level Technical Symposium organized by Geethanjali Institute of science and Technology,Nellore on 19th march, 2015.
- M.Sravanthi (122U1A0482) had participated in the event of paper presentation at the National Level Technical Symposium pragna 2K15 organized by Audisankara Group of Institutions, Nellore on 27th march, 2015.
- M.Jaswanthi (122U1A0481) had participated in the event of paper presentation at the National Level Technical Symposium pragna 2K15 organized by Audisankara Group of Institutions, Nellore on 27th march, 2015.
- M.Sravanthi(122U1A0482) had participated in the event of poster presentation at the National Level Technical Symposium pragna 2K15 organized by Audisankara Group of Institutions, Nellore on 27th march, 2015.
- M.Jaswanthi (122U1A0481) had participated in the event of poster presentation at the National Level Technical Symposium pragna 2K15 organized by Audisankara Group of Institutions, Nellore on 27th march, 2015.
- B.Manasa(122U1A0409) had participated and secured 2nd prize in the event of paper presentation at QIS Fest on 26th and 27th march, 2015organized by QIS Educational Institutions, Ongole.
- B.Venkata Reshma (122U1A0408)had participated and secured 2nd prize in the event of paper presentation.



AY/VOLUME

3D IC technology:

The unprecedented growth of the computer and the Information technology industry is demanding Very Large Scale Integrated (VLSI) circuits with increasing functionality and performance at minimum cost and power dissipation. VLSI circuits are being aggressively scaled to meet this Demand, which in turn has some serious problems for the semiconductor industry. Additionally heterogeneous integration of different technologies in one single chip (SoC) is becoming increasingly desirable, for which planar (2-D) ICs may not be suitable. 3-D ICs are an attractive chip architecture that can alleviate the interconnect related problems such as delay and power dissipation and can also facilitate integration of heterogeneous technologies in one chip (SoC). The multi-layer chip industry opens up a whole new world of design. With the Introduction of 3-D ICs, the world of chips may never look the same again.



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2. Sk.Khajavali, Asst. Professor

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- 2. P.Krishna Kumar (III ECE),
- 3. G. Prasanth(II ECE),
- 4. Sk.Karimulla(II ECE)

2014-15/1



GEETHANJALI INSTITUTE OF SCIENCE AND TECHNOLOGY (Approved by AICTE, New Delhi & Affiliated to JNTU, Anantapur)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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DEPARTMENT/ISSUE